A Simple Wilkinson Power Divider with Harmonics Suppression

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A Simple Wilkinson Power Divider with Harmonics Suppression

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Abstract This article presents a power divider with a simple technique for harmonics suppression. This technique is based on using microstrip open stubs to suppress the second to sixth harmonics simultaneously. This power divider has a simple structure that enables an easy circuit design and analysis. The simulated and experimental results are shown for the proposed 0.9-GHz power divider, which is implemented in microstrip technology. The design equations are derived using the odd- and even-mode formulations.

Keywords harmonic suppression, microstrip, open stubs, Wilkinson power divider

1. Introduction

The Wilkinson power divider was invented in 1960. It is one of the most widely used components in the wireless communication system for power division or combination, such as power amplifiers, mixers, and frequency multipliers (Sun et al., 2011). The main drawback of the conventional Wilkinson power divider is the presence of spurious response due to the adoption of quarter-wavelength transmission lines (Cheng & Ip, 2010).

This problem has been partially overcome (Lin et al., 2007; Woo & Lee, 2005; Zhang & Li, 2008; Yang & Wu, 2008; Yi & Kang, 2003; Tang & Kewei, 2012) by using electromagnetic bandgap (EBG) cells or a defected ground structure (DGS) for harmonics suppression. Unfortunately, these circuits usually require either backside etching or an additional lumped reactive element, which is undesirable for low cost and a mass-production environment (Cheng & Ip, 2010).

Transmission-line stubs elements have been widely used in power dividers for more applications. In Wu et al. (2010a), a transmission-line stub was used in the dual-band Wilkinson power divider, and in Wu et al. (2011), parallel transmission-line stubs were used to improve spurious suppression. In Wu et al. (2010b) and Khalilpour (2011), using

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shunt open stubs with two common methods (Π-shaped and T-shaped open stubs) was investigated. However, in these works, obtaining harmonics suppression with a high level of attenuation is still a subject of discussion and challenge.

Recently, a novel power divider was presented in Cheng and Ip (2010) with spurious harmonic suppression and a simple structure. Compared with this work, the proposed configuration uses a simpler structure and has better performance. The proposed structure has significant advantages in terms of simple topology, which only uses three open stubs and extreme harmonics suppression, which suppresses the second to sixth harmonics simultaneously.

2. Proposed Circuit and Analysis

Figure 1(a) shows the conventional Wilkinson power divider that consists of two quarter-wavelength transmission lines ($\sqrt{2}Z_0$) and an isolation resistor (100 ohms).

The schematic diagram of the proposed power divider is shown in Figure 1(b), which consists of a resistor ($r = 100 \, \Omega$), four similar branch-line sections, and three open-circuited stubs. By applying the even- and odd-mode formulation, the unknown parameters can simply be derived.

![Figure 1. Schematic diagram of power divider: (a) conventional and (b) proposed Wilkinson. (color figure available online)](image-url)
2.1. Odd-Mode Analysis

Assume the circuit is in the odd-mode excitation. Its equivalent circuit is shown in Figure 2. The equations are formulated as

\[ Y_0 = Y_A + Y_B + Y_C, \]  
\[ Y_0 = -j \cot \theta_1 + j \tan \theta_2 + \frac{Z_1 + j \frac{r}{2} \tan \theta_1}{Z_2 + j Z_1^2 \tan \theta_1}. \]  

After simplifications, substituting \( r = 2Z_0 \), then by equating the real and imaginary parts of Eq. (2), the following equations are obtained:

\[ \frac{Z_2}{Z_1} = \tan \theta_1 \tan \theta_2, \]  
\[ \frac{Z_2}{Z_1} \tan \theta_1 - \frac{Z_2}{Z_1} \cot \theta_1 + \tan \theta_2 = \frac{Z_1 Z_2}{Z_0} \tan \theta_1. \]

The comparison of Eqs. (3) and (4) results in

\[ Z_1 = Z_0. \]  

2.2. Even-Mode Analysis

Under even-mode excitation, the proposed power divider’s equivalent circuit can be reduced, as in Figure 3(a), and the \( ABCD \) matrix can be expressed as

\[ \begin{bmatrix} 1 & 0 \\ Y_{eq1} & 1 \end{bmatrix} \times \begin{bmatrix} \cos \theta_1 & j Z_1 \sin \theta_1 \\ j Y_1 \sin \theta_1 & \cos \theta_1 \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ Y_{eq2} & 1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}. \]  

\[ Y_{eq1} = j Y_3 \tan \theta_3 = j \frac{Y_3}{2} \tan \theta_3, \]  
\[ Y_{eq2} = j Y_2 \tan \theta_2 + j Y_1 \tan \theta_1. \]  

Figure 2. Odd mode of power divider. (color figure available online)
The above matrix equation can be expanded to give

\[ A = \cos \theta_1 - \sin \theta_1 \tan \theta_1 - \frac{Z_1}{Z_2} \sin \theta_1 \tan \theta_2, \]  
(9)

\[ B = jZ_1 \sin \theta_1, \]  
(10)

\[ C = \frac{AD - 1}{B}, \]  
(11)

\[ D = -\frac{Z_1}{Z_3} \sin \theta_1 \tan \theta_3 + \cos \theta_1. \]  
(12)

According to Figure 3(b), the new equation for the matrix can be written as

\[ \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_0} & 1 \end{bmatrix} \]  
(13)

\[ Z_{in} = 2Z_0 = \frac{A' + \frac{B}{Z_0}}{C' + \frac{D}{Z_0}}. \]  
(14)
Assuming that the network is reciprocal and lossless (A and D are real numbers; B and C are imaginary), Eq. (14) can be written as

\[ A = 2D, \]  
\[ A^2 - \left( \frac{B}{Z_0} \right)^2 = 2. \]

Equations (15) and (16) can be modified by using Eqs. (9) through (12) to the following:

\[ \frac{2Z_1}{Z_3} \tan \theta_3 - \frac{Z_1}{Z_2} \tan \theta_2 = \tan \theta_1 + \cot \theta_1, \]  
\[ \tan \theta_1^2 = 2. \]

From Eqs. (3), (5), and (18), the following can be written:

\[ Z_2 = \sqrt{2}Z_0 \tan \theta_2. \]  
\[ Z_3 = \frac{Z_0}{2\sqrt{2}} \tan \theta_3. \]

### 2.3. Selection of Circuit Parameters

The unknown parameters of the proposed structure can be calculated by the above equations. The parameter \( \theta_1 \) could be obtained from Eq. (18), which is 55°. The selection of \( \theta_2 \) and \( \theta_3 \) determines the locations of the transmission zeros. Since the nth harmonic suppression is desired, \( \theta_2 \) and \( \theta_3 \) are assigned to be \( \pi/2n \) (Cheng & Ip, 2010). They are obtained as 22.5° and 30°, respectively. The values of \( Z_2 \) and \( Z_3 \) are found to be 30 \( \Omega \) and 10 \( \Omega \), respectively, based on Eqs. (19) and (20). Finally, fine adjustments for physical lengths of the circuit parameters are implemented for better performance.

### 3. Experimental Results

For experimental verification, a 0.9-GHz power divider was fabricated on an RT/Duroid 5880 substrate (Rogers Corporation, Chandler, Arizona, USA) with a relative permittivity of 2.2, thickness of 0.381 mm, and loss tangent of 0.0009, as shown in Figure 4.

The overall dimension of the circuit was about 37.5 mm \( \times \) 30 mm. The S-parameters were measured using an Agilent N5230A network analyzer.

Figures 5 through 8 illustrate the measured and simulated S-parameters of the proposed power divider, in which there is a good agreement between the simulations and measurement results. From Figures 5 and 6, very good input and output matching can be observed. From the experimental results, the input return loss is over 43 dB and output return loss is over 32 dB.

Figure 7 shows the amplitude of transmission parameter \( S_{21} \) in dB; the measured insertion loss is better than 0.3 dB at the center frequency (0.9 GHz). As shown in the figure, the proposed power divider extremely suppresses second to sixth harmonics simultaneously. From Figure 7, the stopband bandwidth (1.4–5 GHz) has been achieved.
Figure 4. Photograph of fabricated power divider. (color figure available online)

Figure 5. Measured and simulated input returns loss of power divider. (color figure available online)
Figure 6. Measured and simulated output returns loss of power divider. (color figure available online)

Figure 7. Measured and simulated insertion loss of power divider. (color figure available online)
with a minimum attenuation level of 20 dB. The measured spurious attenuations are 71, 77, 36, 26, and 34 dB for the second to sixth harmonic frequencies, respectively.

Figure 8 represents the isolation parameter between the two output ports ($S_{32}$). More than 34 dB of port isolation is obtained at the center frequency (0.9 GHz). Moreover, good port isolation is also achieved at harmonic frequencies. As shown in the figure, good agreement between measured and simulated results is achieved.

Table 1 gives the comparison between the proposed power divider and other reported divider topologies.

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4. Conclusion

A new Wilkinson power divider with a novel structure for harmonics suppression is designed, simulated, and measured. The major advantage of the new structure as compared to the previous works is the simultaneous enhancement of suppression of the second to sixth harmonics, which results in the wide stopband bandwidth. The proposed configuration has a simple structure that does not require backside etching or lumped reactive components.

References