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A Broadband Doherty Power Amplifier with Harmonic Suppression

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Abstract

In this paper, the design and implementation of the broadband, Doherty power amplifier (DPA) with 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression, with theoretical analysis is presented. In the proposed structure a novel harmonic suppressed Wilkinson power divider used in DPA, which results in harmonic suppression with high level of attenuation. Moreover the proposed DPA has major advantages in terms of the linearity and works on a wideband frequency range (2.1 – 2.7 GHz) with minimum 40\% drain efficiency (DE). The linearity of the proposed DPA is increased extremely, which significant improvement (7 dBm) is achieved from the main amplifier. In the proposed DPA, the main and the auxiliary amplifiers are implemented using Class-AB and Class -C topology respectively with equal MRF6S27015N MOTOROLA transistors in LDMOS technology.

Keywords: Doherty power amplifier (DPA), harmonic suppression, high efficiency, LDMOS, linearity, matching networks, power amplifier (PA), wideband.

1. Introduction

Nowadays, the rapidly rising power consumption has been occurred by the extensive use of spectrum-efficient modulation techniques, the increasing demand for higher data rates and

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the growing number of wireless communications users. The energy efficiency of base stations should be constantly improved in order to reduce the power loss. Significant energy savings can be achieved by improving the efficiency of the power amplifier (PA) of RF transmitters used in the base station [1]. Different techniques have been proposed to increase the efficiency of power amplifiers. Envelope elimination and restoration (EER) [2], envelope tracking (ET) [3], Doherty amplifiers [4] and varactor-based dynamic load modulation [5] are the most common techniques being proposed. The ease of configuration and the circuit simplicity give the Doherty power amplifier (DPA) many advantages over the other techniques. In DPA, high average efficiency and high linearity are achieved by dynamically adapting the PA load impedance to keep the amplifier in compression during modulation [4-7].

The Doherty amplifier is considered as a solution to enhance the efficiency and linearization [8], [9]. Several approaches have been reported recently to improve linearity [10], [11] and wide operation frequency range of the DPAs [12-21].

Recently harmonic control circuit is used for harmonic suppression in class-F and class-E PAs [22-24] for efficiency improvement, which in these classes harmonic control circuit is the most important block in the power amplifiers design [22]. But so far a few Doherty power amplifiers with harmonic suppression have been reported. In [25],[26] harmonic suppression has been obtained with defected ground structure (DGS) and lumped reactive components in DPAs. Unfortunately, these methods require either backside etching or additional lumped reactive element, which is undesirable for low-cost and mass production environment [27].

In this paper, a novel Doherty power amplifier with wide operating frequency band, high linearity and harmonic suppression is proposed, where a miniaturized harmonic suppressed Wilkinson power divider is used in the DPA structure, which results in 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression with high level of attenuation.
2. Design Process

The basic structure and operation principle of DPAs discussed in this section briefly. The schematic diagram of the conventional DPA is shown in the Fig. 1. The conventional DPA is composed of main and auxiliary power amplifiers. In general, the main amplifier biased for class AB operation, while the auxiliary amplifier has a class C or B bias point to use its low gain at a lower power level [29], in the proposed DPA the main and auxiliary amplifier are biased in class AB and C respectively. The main and auxiliary amplifiers are combined through the quarter-wave transmission line in order to modulate the load impedance of the main amplifier through the current supplied by the auxiliary amplifier into the external load. Other parts of the proposed DPA are an impedance transfer network (ITN), a power divider and matching networks, which will be described in the next sections. In the Fig. 1, $Z_M$ and $Z_A$ are the loads seen by the Main and Auxiliary amplifiers.

2.1. The DOHERTY Amplifier behavioral Analysis

The DPA has two operating conditions as shown in Fig. 2. Low-power region, where only the main device is on and the Auxiliary is kept off and Doherty region, which both devices are active [31].
The analysis of a DPA, starts from the analysis of the current waveforms imposed by the two active devices, according to their biasing level [31]. More in detail, assuming a simplified current source model for the active device, with a constant transconductance ($g_m$) characteristic, a truncated sinusoidal wave shaping can be considered.

### 2.1.1. Analysis in the Low Power Region

In the low power region, only the Main device is operating, and the DPA behaves as a typical Class AB amplifier. The corresponding scheme to be analyzed is shown in Fig. 3. The DPA external load $R_L$ to be selected to assure the maximum drain voltage swing to the main device. Due to simplicity, a maximum voltage swing equal to $V_{Main} = V_{DD} - V_K$, where, $V_{DD}$ is the drain bias voltage and $V_K$, is the device knee voltage, which assumed to be the same for both main and auxiliary devices.
By using the quarter-wave constitutional relationship, the impedance seen by the Main device up to the break condition is given by [32]:

$$ R_{\text{Main}} = \frac{Z_T^2}{R_L} $$

(1)

$$ \alpha = \frac{P_{\text{out Main break}}}{P_{\text{out Main, Max}}} $$

(2)

$$ R_{\text{Main break}} = \frac{2}{I_{\text{Max Main}}} \left( \frac{V_{\text{DD}} - V_{K}}{2} \cdot \frac{1 - \cos \left( \frac{\theta_{AB}}{2} \right)}{\theta_{AB} - \sin \left( \frac{\theta_{AB}}{2} \right)} \right) $$

(3)

where, the $\theta_{AB}$ is the value of the current conduction angle at the end of the low power region.

2.1.2. Analysis in the Doherty Region

In the Doherty region, the scheme to be analyzed is shown in Fig. 4, which both devices are active. The main device can be assumed to behave as a constant voltage source, whose amplitude can be assumed $V_{\text{Main}} = V_{\text{DD}} - V_{K}$.
The overall DPA relevant features, such as the output power, the DC power supplied, and the efficiency respectively, given by the following equations:
\[ P_{\text{out, Main}} = \frac{1}{2} (V_{\text{DD}} - V_K) I_{\text{Main}} \]
\[ P_{\text{dc, Main}} = V_{\text{DD}} I_{\text{dc,Main}} \]
\[ \eta_{\text{Main}} = \frac{P_{\text{out, Main}}}{P_{\text{dc, Main}}} \]  (6)

\[ P_{\text{out, Aux}} = \frac{1}{2} V_L I_{\text{Aux}} \]
\[ P_{\text{dc, Aux}} = V_{\text{DD}} I_{\text{dc,Aux}} \]
\[ \eta_{\text{Aux}} = \frac{P_{\text{out, Aux}}}{P_{\text{dc, Aux}}} \]  (7)

\[ P_{\text{out, DPA}} = P_{\text{out, Main}} + P_{\text{out, Aux}} \]
\[ P_{\text{dc, DPA}} = P_{\text{dc, Main}} + P_{\text{dc, Aux}} \]
\[ \eta_{\text{Main}} = \frac{P_{\text{out, DPA}}}{P_{\text{dc, DPA}}} \]  (8)

### 2.2. DPA Design and Implementation

The proposed DPA is working in the 2.1-2.7 GHz frequency range with 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression. For both main and auxiliary amplifiers, the MRF6S27015N MOTOROLA transistor in LDMOS technology is used.

The DC parameters of the proposed DPA are obtained from the dc I-V curves of the device. The values of the DC parameters are listed in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main DC Bias Current</td>
<td>( I_{\text{DC, Main}} )</td>
<td>150 mA</td>
</tr>
<tr>
<td>Main DC Gate Voltage</td>
<td>( V_{\text{GG, Main}} )</td>
<td>4.3 V</td>
</tr>
<tr>
<td>Auxiliary DC Gate Voltage</td>
<td>( V_{\text{GG, Aux}} )</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Doherty Load</td>
<td>( Z_L )</td>
<td>22.5 - 9.5j Ω</td>
</tr>
</tbody>
</table>

### 2.2.1. Matching Networks
The first step to design the PA is to perform load-pull simulation to find the optimum load impedances at the desired frequency range (2.1-2.7 GHz). Since the efficiency of the Doherty amplifier at the break condition is equal to that of the Class-AB (main) PA [32] and so the proposed DPA works as the broadband amplifier, the load-pull simulation for the main PA are performed to find load impedances at the whole desired frequency range (2.1-2.7 GHz). The resulting optimum load impedances at 2.1-2.7 GHz frequency range are shown in Fig. 5. The optimum load impedance is 22.5 -9.5j Ω at the 2.4 GHz (center of the desired frequency range), while this value at the whole frequency range of the 2.1-2.7 GHz does not have meaningful changes. The exact values of the optimum load impedances in the Fig. 5 are summarized in Table 2.

Table 2: The optimum load impedance values from load pull simulation in desired frequency.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Impedance Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 GHz</td>
<td>23.5-11j Ω</td>
</tr>
<tr>
<td>2.2 GHz</td>
<td>23-10.5j Ω</td>
</tr>
<tr>
<td>2.3 GHz</td>
<td>22.6-10j Ω</td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>22.5-9.5j Ω</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>22.3-9j Ω</td>
</tr>
<tr>
<td>2.6 GHz</td>
<td>22.1-8.5j Ω</td>
</tr>
<tr>
<td>2.7 GHz</td>
<td>22-8j Ω</td>
</tr>
</tbody>
</table>

Figure 5: Simulated optimum load impedances of the main device at 2.1-2.7 GHz frequency range.

2.2.2. Input Power Splitter

Power splitter is one of the most important blocks in DPAs structure. Coupler and power divider are widely used in DPAs, as a power splitter. A novel Wilkinson power divider (WPD) with harmonic suppression is used in the proposed DPA [35]. Fig. 6 shows the
structure of the proposed WPD for 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression, consisting of two quarter-wavelength transmission lines, two branch-lines ($\theta_3$), three open shunt stubs (two $\theta_2$ and one $\theta_1$) and an isolation resistor. The proposed WPD is symmetric, so the odd- and even-mode analyses can be used to determine the circuit parameters for harmonic suppression.

\begin{equation}
251658240
\end{equation}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure6.png}
\caption{Schematic diagram of the proposed power divider [35].}
\end{figure}

\textbf{2.2.2.1. Odd-Mode Analysis}

With referring to the diagram shown in Fig. 7(a), the output admittance of the half-circuit is simply equal to:

\begin{equation}
Y_0 = Y_A + Y_B + Y_C
\end{equation}

where $Y_A$, $Y_B$ and $Y_C$ are admittances of the branch line and stubs in the odd-mode circuit. The real part of (9) becomes:

\begin{equation}
R = 2Z_0(1 - \tan\theta_2 \tan\theta_3)
\end{equation}
where \( R \) is an isolation resistor, \( Z_0 \) is characteristic impedance of a transmission line and \( \theta \) is the electrical length.

while the imaginary part yields:

\[
Z^2 \tan \theta_2 = \frac{R}{2} Z_0 (\tan \theta_2 + \tan \theta_3)
\]

where \( Z \) is impedance of the branch lines and stubs.

Substituting (10) into (11), results in:

\[
Z = Z_0 \sqrt{(\tan \theta_2 + \tan \theta_3)(\cot \theta_2 - \tan \theta_2)}
\]

\[\text{(12)}\]

\[\text{2.2.2.2 Even-Mode Analysis}\]

According to Fig. 7(b) under even mode excitation, the ABCD matrix can be expressed for the equivalent circuit of proposed power divider as follows:

\[
\begin{bmatrix}
\frac{1}{Y \tan \theta_1} & 0 \\
\frac{1}{2} & 1
\end{bmatrix} \times 
\begin{bmatrix}
0 & Y \\
Y & 0
\end{bmatrix} \times 
\begin{bmatrix}
1 & jY \tan \theta_2 \\
Y \tan \theta_2 + jY \tan \theta_3 & 0
\end{bmatrix} = \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix}
\]

\[\text{(13)}\]

where \( Y \) is admittance corresponding to \( Z \).

Subsequently, the ABCD parameters can be obtained as:

\[
A = -(\tan \theta_2 + \tan \theta_3)
\]

\[\text{(14)}\]

\[
B = jZ
\]

\[\text{(15)}\]

\[
C = jY - j \frac{Y}{2} \tan \theta_2 \tan \theta_3 - j \frac{Y}{2} \tan \theta_1 \tan \theta_3
\]

\[\text{(16)}\]

\[
D = -\frac{\tan \theta_1}{2}
\]

\[\text{(17)}\]
The input impedance of the even mode equivalent circuit is expressed as [33]:

\[ Z_{\text{in}} = 2Z_0 = \frac{AZ_0 + B}{CZ_0 + D} \]  \hspace{1cm} (18)

Assuming the network is reciprocal and lossless, then (18) can be written as:

\[ A = 2D \]  \hspace{1cm} (19)

and

\[ A^2 - \left( \frac{B}{Z_0} \right)^2 = 2 \]  \hspace{1cm} (20)

Using (14) - (17), equations (19) and (20) can be modified as follows:

\[ \tan \theta_1 = \tan \theta_2 + \tan \theta_3 \]  \hspace{1cm} (21)

and

\[ \left( \tan \theta_2 + \tan (\theta - \frac{\pi}{2}) \right) - 2 \cdot Z - 2 \cdot Z - 0 \cdot -2 \cdot = 2 \]  \hspace{1cm} (22)
For 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression, $\theta_1$ and $\theta_2$ are obtained to be $\frac{\pi}{4}$ and $\frac{\pi}{6}$ respectively [27]. Substituting these values into (21), $\theta_3$ is obtained, which is $14.1^\circ$. The value of $R$ and $Z$ are obtained from (10) and (11), as 92 and 72 ohms respectively.

The simulation results of the S-parameters for the proposed Wilkinson power divider are shown in Fig. 8. It can be seen from the figure, the power divider works properly at the 2.4 GHz (center of the desired frequency range) and suppressed the 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics with high level of attenuation. Furthermore, as shown in Fig. 8, the simulation results show that the proposed WPD works properly in the frequency range of the 2.1-2.7 GHz.

![Figure 8: The simulated results of S parameters of the Wilkinson power divider for 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression mode.](image)
2.23. Impedance Transformation Network

The impedance transformation network (ITN) is used to transform the output load (50 Ω) to the required impedance value at the DPA common node (C.N.), as shown in Fig. 1. In [32] and [34], it is shown that a transformer with two sections can achieve ideal impedance matching at desired frequency. The shown transformer scheme in Fig. 9, is represented by two transmission lines with electrical lengths $\theta_{M1}$, $\theta_{M2}$ and characteristic impedances $Z_{M1}$, $Z_{M2}$ respectively.

In the proposed DPA, the ITN must transform the standard 50 Ω termination load to approximate $Z_L = 22.5-9.5j$ Ω at 2.1-2.7 GHz frequency range. Fig. 10 shows the simulation result of the designed ITN, which is matched with the value of the optimum load impedances in Table 2. The element parameters of the ITN network are summarized in Table 3.

![Figure 9: Impedance Transformer Network. The load $R_0$ is transformed to a resistance $Z_L$.](image)

$Z_{M1}$, $\theta_{M1}$ $Z_{M2}$, $\theta_{M2}$ $R_0$ $Z_L$
Figure 10: Simulated S-parameters of the ITN.

<table>
<thead>
<tr>
<th>Z_{M1} (Ω)</th>
<th>θ_{M1} (deg)</th>
<th>Z_{M2} (Ω)</th>
<th>θ_{M2} (deg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>54</td>
<td>43</td>
<td>49</td>
</tr>
</tbody>
</table>

3. DPA Implementation and Measurements

The same structure adopted for the main amplifier is replicated for the auxiliary. The main and auxiliary amplifiers connected through the Wilkinson power divider and the ITN at the input and output, respectively. The complete circuit diagram of the proposed Doherty power amplifier is shown in Fig. 11.
The proposed DPA is implemented on Rogers 4003 substrate with $\varepsilon_r = 3.5$ and thickness of 0.508 mm. A photograph of the fabricated proposed DPA, using MRF6S27015N MOTOROLA transistors, is shown in Fig. 12.

Figure 11: Proposed DPA circuit diagram.

Figure 12: Photograph of the fabricated proposed DPA.

3.1 Measurement Results
The Doherty power amplifier is characterized by small-signal and large-signal measurements to evaluate its performance.

### 3.1.1. Small-Signal Measurements

The proposed Doherty power amplifier is characterized in small signal conditions (S-parameters) to verify its frequency behavior. A drain bias of $V_{dd} = 28$ V is used for both main and auxiliary devices. The main amplifier is biased for a quiescent drain current of 150 mA (gate voltage of 4.3 V) while the auxiliary amplifier is biased below pinch-off (gate voltage of 3.3 V). The simulated and measured S-parameters are depicted in Fig. 13, which show the good agreements between simulated and measured results. The input and output matching with $S_{11}, S_{22} < -10$ dB and over than 10 dB gain ($S_{21} > 10$ dB) in the whole frequency range of 2.1-2.7 GHz is obtained. The operation bandwidth, with both input and output matching are smaller than -10 dB and over than 10 dB gain is shaded in Fig. 13. As shown in Fig. 13, the gain of the proposed DPA at 2.4 GHz (center of the desired frequency range) is over than 16 dB.

By implantation of the proposed harmonic suppressed power divider that described above, the Doherty power amplifier with the 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics suppression, with high level of attenuation is obtained.
Large-signal continuous wave (CW) measurements are performed to evaluate the Doherty power amplifier under steady-state conditions. The biasing, as same as the small signal measurement is used in the large signal measurement. Fig. 14 shows measured and simulated, output power and drain efficiency versus frequency of the Doherty power amplifier under a constant input power of 32 dBm. As shown in Fig. 14, the measured output power is higher than 40 dBm in the frequency range of the 2.1-2.7 GHz, with the measured drain efficiency of 40% in the entire desired frequency range. The drain efficiency and output power are maintained higher than 40% and 40 dBm in the 600 MHz bandwidth around the 2.4 GHz, which is shaded in Fig. 14.
Figure 14: Simulated and measured output power and drain efficiency of the DPA versus frequency at a fixed input power of 32 dBm.

The results show that the proposed DPA works as a broadband amplifier. The performance of the proposed Doherty power amplifier is compared with recently reported broadband and harmonic suppressed Doherty power amplifiers in Table 4.

Table 4: Recent Research on Broadband Doherty Power Amplifiers

<table>
<thead>
<tr>
<th>Index</th>
<th>Specification</th>
<th>Frequency Range</th>
<th>BandWidth(MHz)</th>
<th>Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>[11]</td>
<td>40% DE</td>
<td>2.3-2.825</td>
<td>525</td>
<td>GaN</td>
</tr>
<tr>
<td>[12]</td>
<td>N.A.</td>
<td>2.5-2.7</td>
<td>200</td>
<td>GaN</td>
</tr>
<tr>
<td>[13]</td>
<td>30.3% PAE</td>
<td>2.5-2.7</td>
<td>200</td>
<td>HBT</td>
</tr>
<tr>
<td>[14]</td>
<td>40% DE</td>
<td>1.7-2.1</td>
<td>400</td>
<td>LDMOS</td>
</tr>
<tr>
<td>[15]</td>
<td>40% DE</td>
<td>1.65-2.25</td>
<td>600</td>
<td>GaN</td>
</tr>
<tr>
<td>[16]</td>
<td>40% PAE</td>
<td>1.5-2.14</td>
<td>640</td>
<td>GaN</td>
</tr>
<tr>
<td><strong>This work</strong></td>
<td><strong>40% DE</strong></td>
<td><strong>2.1-2.7</strong></td>
<td><strong>600</strong></td>
<td><strong>LDMOS</strong></td>
</tr>
</tbody>
</table>
The proposed DPA exhibits broadband, harmonic suppression and linearity properties at the 2.1-2.7 GHz frequency range, while the reported works in the Table 4, are designed for one purpose. Nevertheless, it can be observed from Table 4, that the proposed DPA has a very good performance.

Fig. 15 shows the simulated and measured power-added efficiency (PAE) and power gain, versus output power at 2.4 GHz. As shown in Fig. 15 the corresponding gain is about 16 dB, which confirms the small signal result. Maximum PAE value is 58% at the output power of 47 dBm.

Fig. 16 shows the measured and simulated output power for main amplifier and Doherty amplifier, versus input power. The results show that the proposed Doherty amplifier extremely increased the linearity of the circuits. The 1 dB compression point (P_{1dB}) for the main amplifier and doherty amplifier are about 38 dBm and 45 dBm, respectively, which 7 dBm improvement is achieved using the Doherty technique.
Figure 16: Measured and simulated output power of the proposed main and Doherty amplifier versus input power.

In the Fig. 17 the measured efficiency for the DPA, Main and auxiliary amplifiers are shown, the measured results confirm the theoretical efficiency behavior of DPA, which shown in Fig. 2. As seen in this figure the proposed DPA achieves over than 62% efficiency.
Figure 17. Measured efficiency for the DPA and both Main and auxiliary amplifiers.

6. Conclusion

In this paper, a design procedure for a harmonic suppressed, broad band and linear Doherty power amplifier, with a theoretical analysis, is presented. The LDMOS transistors are used in the proposed DPA for the both main (class-AB) and auxiliary (class-C) amplifiers. The small and large signal measurements confirm that the proposed Doherty power amplifier
has major advantages in terms of high linearity, wide operation frequency band and harmonic suppression, simultaneously. The proposed DPA shows the good performance on the 2.1-2.7 GHz frequency range with minimum 40% drain efficiency and suppresses the 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics of this frequency range with high attenuation level. Moreover, the proposed DPA, extremely improved the linearity of the main amplifier.

References


Highlights:

- A novel Doherty power amplifier (DPA) is designed, simulated and fabricated.
- A novel harmonic suppressed Wilkinson power divider is used in the proposed DPA.
- The DPA has advantages of linearity, UWB and harmonic suppression, simultaneously.
- The small and large signal measurements confirm the simulation results.